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Perspective

Semiconductor Nanowires: A Chemical Engineering Perspective

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Introduction

Semiconductor nanowires exhibit a variety of unique material properties, including mechanical flexibility, size-dependent optical and electronic properties, and solution processability. There have been many recent proof-of-concept laboratory demonstrations of new technologies employing semiconductor nanowires. In order for these concepts to make it to the marketplace, chemical engineers are needed to develop industrial scale chemical processes for nanowires. This review describes fundamentals of nanowire synthesis, processing, and some of the promise of applications.

Semiconductor nanowires[1] are threadlike *crystals* with nanometer-scale widths and lengths that can be more than a millimeter. A diameter of a few nanometers corresponds to only about 10 atomic planes, and nanowires can have remarkably high-surface area-to-volume ratios. For example, one gram of 10 nm dia. Si nanowires stretched end to end would wrap around the earth more than 130 times. Figure 1 shows some examples of semiconductor nanowires. The unique chemical and physical properties of semiconductor nanowires are unlike those of any other material found in nature. Like most polymers, nanowires are a creation of chemistry and must be synthesized in the laboratory.

Many possible applications for nanowires exist, including new functional composites, membranes, printed electronics and fabrics, which require large amounts of nanowires. Commercialization will require reactor systems that can produce nanowires at production rates of more than tens of kilograms per day, and, therefore, robust synthetic schemes are needed that can be scaled to an industrial setting. There is currently no existing example of an industrial-scale nanowire production process. Once nanowires are made, they require handling and processing: for example, purification, post-synthesis chemical modifications, deposition on supports, molding into fibers or membranes, or the incorporation with other materials as composites. A tremendous amount of chemical processing development is needed before nanowire technologies can become a commercial reality.

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Synthesis

The Chemical Approach. Various strategies exist for generating semiconductor nanowires, including lithographic patterning and fabrication,[2] templated crystallization,[3] sacrificial substrate "printing",[4,5] and chemical synthesis.[1,6–8] The earliest semiconductor nanowires were made using microfabrication techniques developed for the microelectronics industry and were electrically isolated heterostructures fixed to substrates that were extremely expensive and time-consuming to make.[2] Chemists were beginning to develop the chemical synthesis of "free-standing" semiconductor nanostructures, like semiconductor quantum dots, in the 1980s.[9] The underlying concept was to avoid *top-down* microfabrication techniques and to rely instead on *bottom-up* molecular assembly to make semiconductor nanostructures.

In the 1990s, examples of nanowires made by chemical routes were appearing. Canham discovered photoluminescence in Si nanostructures using an electrochemical etching process,[10] and Martin and others demonstrated the use of mesoporous templates like anodized alumina membranes to synthesize nanowires.[3] Chemical routes were producing arrays of vertically-aligned nanowires, which was impossible using lithographic patterning and deposition microfabrication techniques. The chemical synthesis of the carbon nanotubes provided an additional proof-of-principle that nanowire-like structures could be generated from simple reactants using a chemical approach.[11]

The chemical synthesis of many types of semiconductor nanowires has now been demonstrated.[1] In fact, some semiconductors like ZnO spontaneously form nanowires under various controlled crystallization conditions.[7,12] The wurtzite crystal structure of ZnO induces nanowire formation, which occurs by simply evaporating and condensing ZnO or by precipitation from aqueous salt solutions.[7,12] Other examples of semiconductors that can spontaneously form nanowires include Bi_2S_3 and $Pb_3O_2Cl_2$.[1] Ultranarrow nanowires, with

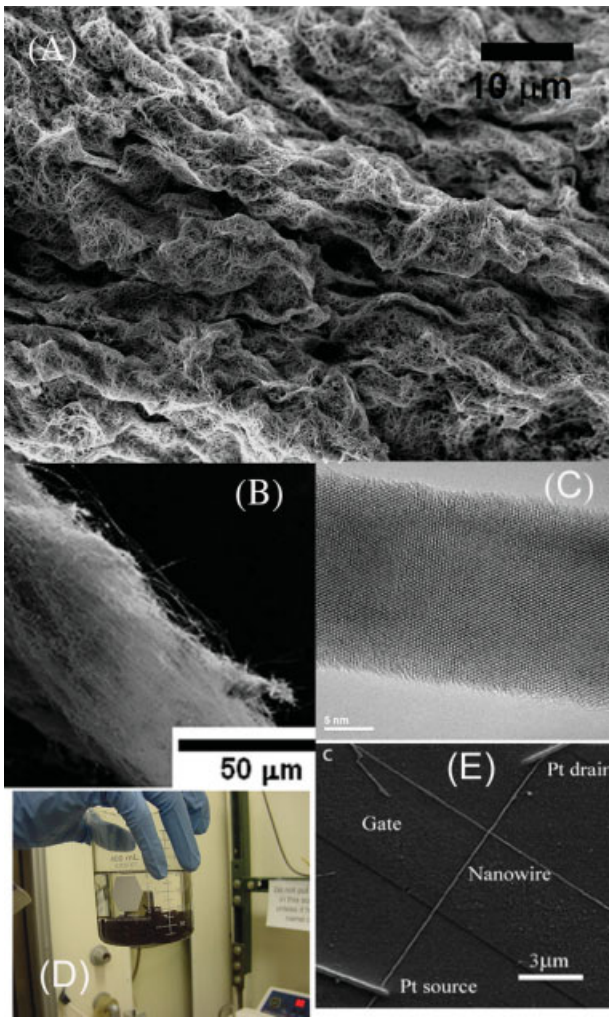

Figure 1. Images of semiconductor nanowires: (A) SEM image of a mat of SFLS-grown Si nanowires; (B) SEM image of wool-like Ge nanowires; (C) TEM image of a Ge nanowire showing its internal crystallinity; (D) a beaker of ~1 g of Ge nanowires, and (E) SEM image of a single Ge nanowire FET structure.

sub-5 nm dia., have also been made by "directed" spontaneous nanowire growth by utilizing surfactants and carefully controlled reactant decomposition kinetics. Nanowires of CdSe and CdS for example, with diameters of less than 2 nm, and aspect ratios greater than 100 have been made in this way.[13,14] The oriented attachment of nanocrystals in solution has provided another spontaneous route to nanowire growth, which has been demonstrated for some materials with cubic crystal structure, including CdTe and PbSe.[15,16]

Most semiconductors, however, require coaxing to form nanowires. One of the most successful and general methods for generating semiconductor nanowires is the vapor-liquid-solid (VLS) approach, first reported in 1964 by Wagner and Ellis.[17] This method relies on the use of a metal that forms a eutectic with the semiconductor of interest to seed nanowire growth. "VLS" describes the progression of semiconductor atoms from *vapor* phase reactants fed into the system to the *liquid* metal: semiconductor solution that forms when the reaction temperature is above the metal: semiconductor eutectic temperature to the *solid* nanowire that grows as semiconductor is continuously fed to the system. Au and Si for example form a eutectic at ~360°C, which, thus, sets the lower limit to the temperature needed for Si nanowire growth. The reaction temperature must also be sufficient to decompose the reactant. The VLS method has been used to grow nanowires of many different kinds of semiconductors, including Group IV, III-V and II-VI compounds, with controlled diameters less than 100 nm.[1]

The key to diameter control using the VLS approach is the use of nanoscale metal seed particles.[18] In this size range, each seed particle leads to only one nanowire, with a diameter that nearly matches the seed particle diameter. The nanowire diameter can be tuned by first synthesizing the seed particles with the desired size and then inputting them into the reactor.[8,18] Nanowires with controlled diameter can also be produced by VLS growth off a substrate coated with a thin layer of seed metal.[19] The seed metal film dewets from the substrate at the nanowire growth temperature to form nanosize droplets that seed nanowire growth.

VLS growth has been carried out in various configurations, from laser ablation[20] to chemical vapor deposition (CVD),[19,20] and chemical beam epitaxy (CBE).[8] CVD-VLS and CBE-VLS provide very powerful techniques for making high-quality semiconductor nanowires with controlled diameter that are interfaced intimately with substrates. However, one problem with these methods is that the total yield of nanowires is quite small since growth is limited to the substrate. The process is nearly ideal for nanowires integrated into microelectronic device structures fabricated using standard microelectronics processes, as nanowires can be grown in place under conditions of very high-chemical purity; however, for applications that require large quantities of nanowires, like polymer-nanowire composites for structural applications or nanowire fibers for textile applications, the CVD-VLS process may not be applicable. Nevertheless, there have been recent efforts toward scaling up the VLS process by using mesostructured supports infused with catalyst particles.[21]

Solution-phase synthetic methods for nanowires provide promising alternatives to vapor-phase synthetic routes for the industrial-scale manufacture of semiconductor nanowires. Buhro first demonstrated the synthesis of InP, InAs and GaAs nanowires in solution by a VLS-like growth from low-melting metal seeds of In and Ga at approximately 200°C.[6] This "solution-liquid-solid" (SLS) growth process has since been applied to many different semiconductor nanowires with controlled diameter.[6] SLS growth is only limited by the boiling temperature of the solvent, which must exceed the eutectic temperature of the metal: semiconductor combination (for Au:Si and Au:Ge for example, these eutectics occur at about 360°C). Solvents are available with very high-boiling points, and Si nanowires were produced by SLS growth recently using Au nanocrystals as seeds.[22] One way to reach higher-reaction temperatures in solution is to pressurize and heat the solvent above its critical point.[18] For example, toluene can be heated up to 450°C under pressure (i.e., 100 ~ 300 bar), and used as a solvent medium to carry out nanowire synthesis. This "supercritical fluid-liquid-solid" (SFLS) approach

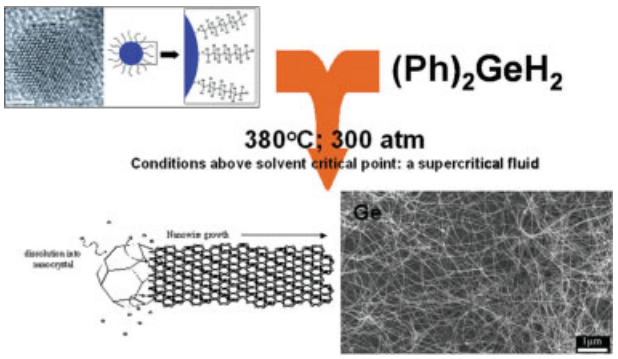

Figure 2. Schematic illustration of the SFLS process: colloidal gold nanocrystals are synthesized with the desired diameter and fed into the supercritical reactor with the reactant, in this case, diphenylgermane (DPG).

DPG decomposes to Ge atoms, which dissolve into the Au nanocrystal to form a liquid Au: Ge droplet that becomes saturated with Ge, and then extrudes a crystalline Ge nanowire.

(Figure 2) to nanowire growth has also been applied to a variety of semiconductors, including Si, Ge, GaAs and GaP and scaled up to gram-scale quantities in single reactions.[1]

Surface Chemistry and Impurities. The nanowire surface can be modified chemically to improve their materials characteristics, like stability and processability, and to enhance their functionality. Chemical routes have been developed to deposit inorganic shells or to graft chemically-bonded organic ligands on nanowire surfaces. Because most semiconductors are susceptible to oxidation (Ge and Si for example), semiconductor nanowires generally require surface passivation to prevent their corrosion, particularly if they are to be used in harsh oxidative environments.[21,23] For electronic and optoelectronic applications, surface passivation is particularly important because the surface can host traps for charge carriers.[24] For example, surface traps can lead to very poor performance in field effect transistor (FET) applications. In a FET, trapped charge unpredictably contributes to the electric field of the gate electrode and changes the device response over time, leading to time- and history-dependent device characteristics. These trap states, or "slow surface states," correspond to chemical defects, like dangling bonds or other chemical impurities, that can be eliminated to a significant extent by effective chemical surface passivation with organic ligands.[21,23–25] For example, hydrocarbon monolayers can be tethered covalently to Ge and Si surfaces by hydrogermylation or hydrosilylation reactions with alkenes.[21,23–25] For Ge nanowires, alkanethiols have been shown to be excellent passivation molecules. The organic ligand passivation of Si and Ge nanowires has exhibited surprisingly good resistance to oxidation,[21,23] and provides one way to obtain chemically and electrically robust nanowires for electronic and optoelectronic applications.

Inorganic coatings have also been applied rather widely to semiconductor nanowires to achieve chemical passivation and in some cases, added functionality. The influence of the surface curvature on the quality of inorganic interfaces is not well understood. For example, can a really good, trap-free, thermal oxide be grown on a semiconductor nanowire with its highly curved surface? What are the best strategies for obtaining conformal epitaxial coatings on nanowires? What is the maximum strain that can be accommodated between a nanowire core and a shell material without the formation of dislocations or other defects? These remain open questions. However, many examples exist in the literature of nanowires coated with inorganic shells that have exhibited outstanding electrical properties, indicating that the chemical interface is nearly perfect.[25] For example, core/shell heterostructure nanowires have been formed by two-step core synthesis and shell coating procedures, including homoepitaxial growth of B-doped Si shells on intrinsic Si and heteroepitaxial growth of Ge/Si, Si/Ge and Ge/Si/Ge core-shell and core-shell-shell structures. InAs/InP core/shell nanowires with extremely high mobililties — up to 11,500 cm^2/V sec — have also been formed.[25] Ge/Si nanowire heterostructures also were reported to exhibit extremely good transistor device characteristics. Ge nanowires coated with a dielectric layer (Al_2O_3), and a second coating of Al metal have also been fabricated, which are suited for "surround-gate" FET architectures.

Only a rudimentary understanding of impurities in semiconductor nanowires exists. For instance, it is not well established what kinds of impurities exist in nanowires, where they are located and how they affect the properties of the nanowires. For high-performance electronic devices, dopant impurities must be added to the nanowires to induce n- and p-type behavior. Nanowire doping has been achieved during the VLS growth process by adding a reactant like diborane to the Si nanowire growth process.[25] However, the location of the dopant atoms in the nanowire remains poorly understood, and there is some evidence of dopant migration out of the nanowire into the surface. Dopant can also incorporate into the nanowire by sidewall deposition during nanowire growth. As an alternative to *in situ* doping, Ho and coworkers recently demonstrated Si nanowire doping by adsorbing organic monolayers with either B or P dopant atoms, followed by a rapid thermal anneal to drive the dopant into the core of the nanowire.[26] Boron doping was achieved by adsorbing alkylboronic acid pinacol ester to the Si surface by a thermally-promoted hydrosilylation, followed by a thermal anneal to drive the dopant into the nanowire core. The dopant concentration is self-limiting using this process, since the dopant concentration on the nanowire surface is limited to monolayer coverage. N-type doping with phosphorus was also demonstrated by using either diethyl 1-propylphosphonate (DPP), or trioctylphosphine (TOP), as the monolayer molecule. In-place doping by low-energy ion implantation has also been shown to be an effective way to control dopant concentrations in nanowire FETs.[27]

The role of unwanted impurities and their effect on the electronic properties of semiconductor nanowires is also poorly understood. Gold has been shown to migrate along nanowire surfaces during CVD-VLS growth, but this migration depends strongly on the growth conditions. Under CVD conditions with reasonable growth rates, Au does not appear to migrate along the nanowire surface.[28] New analytical tools, like state-of-the-art electron microscopy with elemental mapping capability with nearly atomic resolution, have been developed and Au atoms have been mapped in Au-seeded CVD-VLS grown nanowires.[28] Understanding what happens

to the Au seeds during VLS-like nanowire growth is particularly important for FET applications because gold forms deep electronic traps in Si (and Ge), and significantly decreases transistor performance. Nonetheless, there are many demonstrations of gold-seeded Si nanowires that have exhibited good transistor device characteristics. Alternative metals have also been used to seed nanowires, including Ni, Co, Fe and Cu.[29]

Nanowire Heterostructures. Axial heterostructures have been made by CVD-VLS by alternating reactants.[1,25] Nanowires with quantum dot-like quantum wells can be made by choosing materials with the appropriate band offsets. Due to their very thin diameter, heterojunctions between materials with large lattice mismatches can be made without the formation of dislocations. For example, axial Si/Ge and InAs/InP heterojunctions have been incorporated along the length of nanowires without defects. This opens exciting possibilities for creating materials with new physical properties, and also for studying previously unexplored physics. Dopant concentrations can also be modulated along the length of nanowires, giving rise to nanowires with internal *p-n* junctions for either electron-hole separation (as in photovoltaics) or recombination (as in light emitting applications).

Applications

Transistors. Semiconductor nanowires are being explored for making higher performance transistors that can be combined with Si CMOS (complementary metal-oxide-semiconductor) integrated circuits (ICs), and as a printable media for a new class of thin film transistors (TFTs).[25] Nanowires have the potential to improve transistor performance relative to the state-of-the-art and to add functionality like light weight, mechanical flexibility and transparency.[5,25] Semiconductor nanowires could also enable heterogeneous integration of different devices and materials on ICs, for example, as switchable light sources for optical integration and chemically-gated sensor circuits. The nanowire transistor is fabricated by positioning nanowires between source and drain electrodes. The electrical current passing through the nanowire is modulated by a neighboring gate electrode. Fabrication of the nanowire transistor requires chemical processes for nanowire synthesis, and methods for manipulating and integrating nanowires into device structures. Radically new fabrication strategies are being developed to achieve this, including *bottom-up* nanowire self-assembly and solvent-based deposition strategies.

In one effort, nanowires are being explored as the basis for new ultrahigh performance FETs. These applications require fabrication under carefully controlled environmental conditions with high purity. New device fabrication strategies are needed because the architectures are quite different than the conventional planar Si CMOS device. For example, one promising device is the short channel, vertically-aligned, wrap-around gate FET, which has the potential to significantly lower FET power consumption. Functioning vertical FETs have been made and tested with good device response. For example, vertical short channel Si nanowire FETs have also been fabricated with subthreshold slopes as low as 6 mV/decade-an order of magnitude less than the fundamental limit of a Si CMOS device.[30]

Semiconductor nanowires are also being explored as a new solution-processable, printable electronic material for thin film transistors (TFTs) as an alternative to amorphous silicon (a-Si). The performance of a-Si TFTs is limited by carrier mobilities of only $\sim$1 cm^2/V sec for a-Si. Nanowire FETs have been reported with carrier mobilities more than two-orders of magnitude better than this.[25,31] Nanowires also have the advantage over a-Si in that they are mechanically flexible and can be deposited onto substrates at room-temperature by casting from solvent dispersions. For practical applications, the drive currents of single nanowire FETs are much too low and therefore a common approach to fabricating nanowire FETs is to construct them with an array of multiple, parallel-aligned nanowires. This geometry requires new fabrication and nanowire growth approaches, as multiple nanowires must be contacted and gated simultaneously. Nanowire TFTs have been constructed on various substrates, including glass and plastic, with good device performance; for example, TFTs of p-doped Si nanowires have exhibited field effect mobilities as high as 119 cm^2/V sec, a subthreshold swing of 600 mV/decade, and threshold voltages less than 1 V.[31] These mobilities are about two-orders of magnitude better than the best organic semiconductors that have been explored for TFT applications.[32] Compared to organics for FETs, nanowires are single crystals of inorganic semiconductors that do not have grain boundaries between the source and drain electrodes. Nanowires can also be doped either n- or p-type with impurities. One challenge facing commercial nanowire TFT fabrication is the need for a scalable nanowire deposition method. Nanowires must be densely packed and aligned in the channel of the device for good performance. Routes developed for aligned nanowire deposition from solvent dispersions include flow-alignment, Langmuir-Blodgett alignment and transfer, and a blown-bubble method.[25] It is not clear that any of these methods can achieve the reliability and throughput needed for an industrial process, and new nanowire deposition schemes are still being sought.

Despite the number of articles that have reported prototype semiconductor nanowire FETs with extremely good device characteristics — far better than a-Si TFTs — there are still no commercial products. Part of the reason for this is the need to better understand the fundamental limitations of nanowire performance in FETs, as well as the need for inexpensive and scalable processes for nanowire synthesis, processing and device fabrication. Due to subtle differences in nanowire synthesis and processing, there have been widely varying reports of electron and hole mobilities in nanowire FETs, ranging from extremely high values that are better than bulk single crystals, to very poor mobilities. The field effect mobility depends on various factors, including the quality of the source/drain contacts, impurities, electrostatic coupling between the gate electrode and the nanowire and trapped interfacial charge, which depend on how the device is fabricated. Furthermore, the field effect mobility can depend on gate and source-drain voltages as well. Traps can dominate the field effect mobility for small voltages, but then when the traps are filled at high voltages, the field effect mobility of the device can increase significantly. Surface modification has been demonstrated to significantly influence the properties of nanowire FETs.

Brittle and Flexible. . .Crystals With No Grain Boundaries. Semiconductor nanowires are made from materials that are brit-

tle, but they are very flexible because of their small size.[33,34] Nanowire cantilevers have been made and studied as the basis for new nanoelectromechanical resonators (NEMS). One of the challenges with NEMS cantilevers is the apparent decrease in mechanical quality factor Q, with decreasing diameter. Q is a measure of the relative energy stored in the cantilever compared to the energy dissipated per cycle, and for most applications a high Q value is desired. Therefore, the lowering of Q with decreasing cantilever diameter is not desirable, and furthermore, the reasons behind this lowering of Q are poorly understood. Surface losses dominate Q at smaller diameter, but there is not a detailed molecular understanding of these energy loss processes. The size dependence of the elastic modulus of a semiconductor nanowire with narrow diameters (i.e., less than ~10 nm) is also not well understood. However, the nanowires are clearly flexible, which makes them ideally suite for applications like flexible FETs. Also, because the nanowires do not have grain boundaries, they exhibit an ideal strength before fracture that is a couple of orders of magnitude higher than bulk crystals.[34] These unique mechanical properties should make it possible to apply crystalline semiconductor materials in entirely new contexts, such as electronic and optoelectronic fabrics.

Thermoelectrics. Thermoelectric materials enable the direct conversion of waste heat into electrical power, or electrical power into heating or cooling.[35] Thermoelectric devices could alleviate the need for refrigeration coolants and could harvest waste heat in automobiles or chemical plants for electrical power. Thermoelectrics have a wide range of potential applications, but their practical use has been limited by the lack of materials with adequate thermoelectric figure of merit $ZT = \sigma S^2 T/\lambda$ where σ, S, T, and λ are the electrical conductivity, the Seebeck coefficient, the average temperature and the thermal conductivity. ZT of 1 or higher is considered good.

Semiconductor nanowires have been explored as a materials platform for obtaining high ZT. ZT is affected by the dimensions of the material and recently, ZTs rivaling those of the best existing materials were reported for Si nanowires with rough amorphous surfaces.[35] Bulk Si is not a good thermoelectric material, so these results have provided recent inspiration in the search for nanowires with very high ZT. Nanomaterials have shown promising results in the laboratory, but these results thus far have not translated to practical device applications. One of the challenges is the need for large quantities of semiconductor nanowires with the desired properties.

Self-Powering Devices. There are many electronic applications that require self-powering capability, as in the case of space applications or biomedical devices placed within the body, like pace makers. Any electronic device that requires a battery that is difficult to replace is a good candidate for self-powering capability. Semiconductor nanowires have been shown to have unique piezoelectric properties that could be applied to the creation of new nanogenerator technologies.[36] When a stress is applied to the nanowire, an electric field is generated that can be harvested to power electrical devices. ZnO nanowires and even Si nanowires have exhibited strong piezoelectric effects. Nanogenerators and nanopiezoelectrics based on arrays of ZnO nanowires have been demonstrated, and the voltage generated by a nanowire deformed by a lateral force appears to be enough to drive an FET.[36]

Chemical Sensors. Chemical sensors are being made using semiconductor nanowires. The sensors are essentially *chemically-gated* transistors. The very high-surface area-to-volume ratio of the nanowires makes their conductivity highly sensitive to environmental species. In the case of TFTs, this may be a problem that requires special packaging to deal with in order to ensure reproducible and robust transistor behavior. However, for chemical sensing, this sensitivity is the property that is being exploited. Semiconductor nanowires have been used as chemical sensors for a variety of analytes, from small molecules to pH to biomolecules to cells.[4,25]

Si and Ge Nanowire Mesh Anodes for Li-ion Insertion Batteries. Si (and Ge) nanowires have been tested as potential replacements to carbon in Li ion batteries. The Li ion battery has widespread commercial use, but could be greatly improved by developing new electrode materials with higher Li storage capacity. Commercial Li-ion insertion batteries rely on graphitic carbon as the anode material with Li intercalating between graphitic sheets, and the maximum amount of Li that can be stored corresponds to a maximum storage capacity of 372 mAh/g. Si and Ge form a variety of Li-rich intermetallic compounds and alloys, like Li_xSi and Li_xGe. The maximum Li storage capacity of Si is nearly an order of magnitude higher than carbon. For example, $Li_{22}Si_5$ ($Li_{4.4}Si$) has a theoretical Li storage capacity of 4,200 mAh/g, which is more than one-order of magnitude higher than the Li storage capacity of carbon (372 mAh/g). One problem with using Si as a Li insertion storage material is its large volume increase (by 400%) when large amounts of Li are incorporated, leading to pulverization. Si or Ge nanowires might be able to accommodate these dramatic volume expansions without cracking. The extremely high-surface area of the nanowires also enables the solid-state transformations to occur without significant kinetic limitations (i.e., solid state Li diffusion into the Si volume). Recently, Cui showed that Si nanowires could indeed by used as an anode material for Li-ion insertion batteries and demonstrated very high-capacity and decent cycling stability.[37]

Surface and More Surface: Superhydrophobic Properties and Nanowire Membranes. With the ability to synthesize large amounts of nanowires, applications like nanowire paper, membranes and fibers, are being developed. The nanowires are purified and then formed into nonwoven materials. Stellacci recently demonstrated the use of such nanowire paper as a unique membrane material for absorbing oils and other specific solvents.[38] They synthesized $K_{2-x}Mn_8O_{16}$ nanowires using a hydrothermal process. The hydrothermal process is critical because it produced sufficient nanowires to form macroscopic membranes. The nonwoven mats of nanowires were found to absorb solvents of up to 20 times the weight of the membrane due to capillary forces and the wetting properties of the solvent for the substrate. The nanowire surface chemistry could be modified to be hydrophilic or hydrophobic to determine the solvents that would be absorbed by the membranes. The nanowires modified to be hydrophobic for example, were found to be *superhydrophobic*. By further modifying the nanowire surfaces with functional molecules, they might be used to form membrane materials with more functionality to absorb environmental pollutants like no other known material. However, since the nanowires are an inorganic material, they exhibit very good thermal stability-unlike polymer membranes, which decompose at relatively low-temperature.

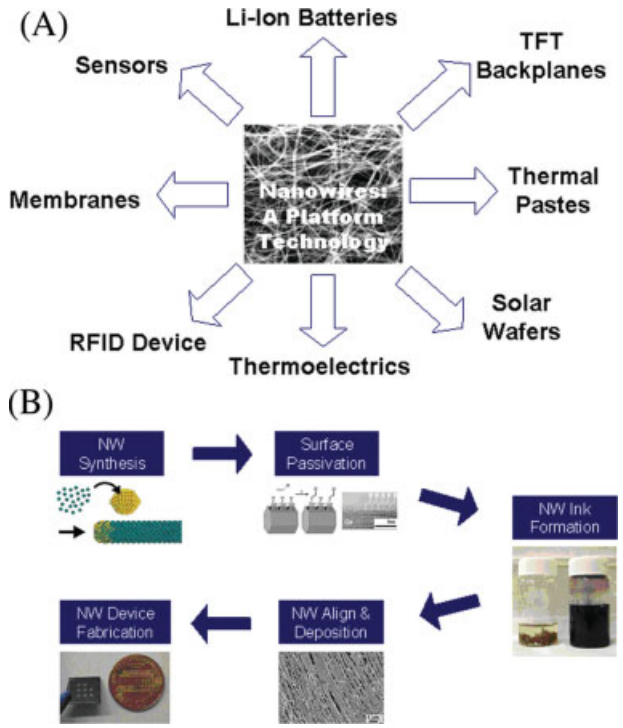

Figure 3. (A) Semiconductor nanowires are a platform materials technology with a wide variety of potential applications, ranging from transistors to sensors to solar cells, and (B) Illustration of the process flow for printed nanowire TFTs.

Scaffolds for Photovoltaic Devices. Semiconductor nanowires are being explored as new materials for solar cells or photovoltaics (PVs). Undeniably, one of the most pressing societal challenges is the need for renewable energy sources that do not add to the atmospheric carbon content. The sun provides a nearly infinite source of energy. However, new solar cell technologies are needed because existing approaches are too expensive. The most successful commercial photovoltaics technology is polycrystalline Si. Polycrystalline solar cells have good efficiencies and are durable, but they are expensive to produce. To compete with coal for example, the cost/kWh needs to be ~\$0.04/kWh, which is currently more than an order of magnitude less than the cost/kWh of PV-generated power. New materials systems are being sought that can lower the manufacturing costs of PVs by an order of magnitude or more, while still achieving power conversion efficiencies (PCEs) greater than 10% and good durability. This is a daunting challenge. Alternatives to Si and vapor-deposited solid-state thin film technologies (like CdTe, a-Si, and Cu(In, Ga)Se_2 (CIGS)) are being sought, such as the use of organics. The problem with organics is their very short electron-hole diffusion lengths, and, therefore, strategies involving mesostructured PV electrodes in which the hole and electron transport layers are "folded" into the volume of the absorber layer are being explored. Electrodes structured in the form of nanowires seem to be a perfect solution, as large interfacial area can be generated, and the nanowires form ideal crystalline pathways for carrier transport.[39,40] Arrays of ZnO nanowires have been infused with organic dyes and light-absorbing nanocrystals to make functional PVs.[39] The power conversion efficiencies (PCEs), however, have been relatively low—much less than the 10% that is needed to have a chance at commercialization. Better understanding is needed of electron-hole separation at the nanowire surface, charge trapping and transport down the nanowire length in a functional PV, and of how best to fabricate the structures with low cost and the fewest defects possible.

The Path Forward

Nanowires have tremendous technological potential (Figure 3). They offer a suite of properties not found in any naturally occurring materials. Nanowires are a product of chemistry, and industrial chemical processes are ultimately needed to transfer them to the commercial sector. Chemical engineers are needed to develop these processes and will undoubtedly play a fundamental role in the future success of the nanowire field.

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